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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/864,698	05/23/2001	David J. Corisis	3070.2US (96-1079.2)	1726

24247 7590 10/24/2002

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EXAMINER
GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/864,698	Applicant(s) CORISIS ET AL.
	Examiner David E Graybill	Art Unit 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☒ Claim(s) *1-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8-21-2 has been entered.

Claims 1-17 are objected to because in claim 1, penultimate line, the term "frame." is grammatically incorrect.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1 the limitations, "a first voltage reference plane to overlie in immediate proximity therefrom," and, "said first group of lead fingers and in isolation," are incomprehensible in their contexts.

In claim 1 there is insufficient antecedent basis for the language, "said first side of said die-attach location," "said first group of lead fingers extending from said first side of said die-attach location," "said second opposing side of said die-attach location," and, "said second group of lead fingers extending from said second opposing side of said die-attach location."

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-10 and 13-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Lee (5089878) and Farnworth (5012323).

At column 2, lines 1-47, column 3, line 1 to column 4, line 51, and column 6, lines 37-66, Lee teaches the following:
1. A semiconductor die assembly comprising: a semiconductor die 2 having a plurality of bond pads on an active surface thereof; a lead frame 8 having at least a first group of lead fingers 12 and a second group of lead fingers 12 to respectively extend from first and second opposing sides of said semiconductor die attached to a die-attach location 10 on said lead frame to another side of said lead frame in a substantially mutually parallel configuration [at least at outer ends of lead fingers 12]; a first voltage reference plane 18b to overlie in immediate proximity to therefrom, said first voltage reference plane overlying at least a portion of said first group of lead fingers extending from said first side of said die-attach location

toward said another side of said lead frame; and a second voltage reference plane 18b to overlie in immediate proximity to said second group of lead fingers and in electrical isolation therefrom, said second voltage reference plane overlying at least a portion of said second group of lead fingers extending from said second opposing side of said die-attach location toward said another side of said lead frame. said first group of lead fingers and in electrical isolation.

3. The assembly of 1, wherein said first voltage reference plane and said second voltage reference plane are adhered to at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

4. The assembly of 3, wherein said first voltage reference plane and said second voltage reference plane are adhered directly via a non-conductive adhesive 36 to said at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

5. The assembly of 1, further comprising a packaging material 34 encapsulating at least said active surface of said semiconductor die.

6. The assembly of 5, wherein said packaging material at least partially covers said first and said second voltage reference planes and said first and said second groups of lead fingers.

7. The assembly of 1, wherein said lead frame includes a die-attach paddle 10 to which said semiconductor die is attached.

8. The assembly of 1, wherein said die-attach location comprises a die-attach paddle.

9. The assembly of 1, wherein said first voltage reference plane and said second voltage reference plane are electrically connected to at least one lead finger of said first group of lead fingers and said second group of lead fingers, respectively, which in turn is connected through a bond pad to a reference potential of said semiconductor die.

10. The assembly of 1, wherein at least one of said first voltage reference plane and said second voltage reference plane includes projections extending away from a direction of said immediate proximity of said first group of lead fingers and said second group of lead fingers, respectively.

13. The assembly of 1, wherein said first voltage reference plane and said second voltage reference plane are of sufficient mass to measurably alter heat transfer characteristics of said assembly.

14. The assembly of 1, further comprising a packaging material encapsulating said assembly so that only outer ends of said at least said first group of lead fingers and said second group of lead fingers extend therethrough.

15. The assembly of 1, wherein said first voltage reference plane and said second voltage reference plane extend over at least about fifty percent of a surface area of said at least said first group of lead fingers and said second group of lead fingers, respectively.

16. The assembly of 1, wherein said first voltage reference plane and said second voltage reference are separated from said at least said first group of lead fingers and said second group of lead fingers, respectively, by an insulating adhesive structure.

17. The assembly of 16, wherein said insulating adhesive structure comprises an insulating film 36 having an adhesive on opposing surfaces thereof, one surface of said opposing surfaces being adhered to at least one of said first group of lead fingers and said second group of lead fingers and another surface of said opposing surfaces being adhered to at least one of said first voltage reference plane and said second voltage reference plane.

18. A lead frame to be assembled to a semiconductor die comprising: a lead frame having at least a first group of lead fingers and a second group of lead fingers to respectively extend from first and second opposing sides of an intended die-attach location 10 to another side of said lead frame in a

substantially mutually parallel configuration; a first voltage reference plane to overlie in immediate proximity said first group of lead fingers and in electrical isolation therefrom, said first voltage reference plane overlying at least a portion of said first group of lead fingers extending from said first side of said intended die-attach location toward said another side of said lead frame; and a second voltage reference plane to overlie in immediate proximity said second group of lead fingers and in electrical isolation therefrom, said second voltage reference plane overlying at least a portion of said second group of lead fingers extending from said second opposing side of said intended die-attach location toward said another side of said lead frame.

19. The assembly of 18, wherein said first voltage reference plane and said second voltage reference plane are adhered to at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

20. The assembly of 19, wherein said first voltage reference plane and said second voltage reference plane are adhered directly via a non-conductive adhesive to said at least some of the lead fingers of said first group of lead fingers and said second group of lead fingers, respectively.

21. The assembly of 18, wherein said lead frame includes a die-attach paddle 10 to which said semiconductor die is attached.

22. The assembly of 18, wherein said die-attach location comprises a die-attach paddle.

23. The assembly of 18, wherein at least one of said first voltage reference plane and said second voltage reference plane includes projections extending away from a direction of said immediate proximity of said first group of lead fingers and said second group of lead fingers, respectively.

24. The assembly of 18, wherein said first voltage reference plane and said second voltage reference plane extend over at least about fifty percent of a surface area of said at least said first group of lead fingers and said second group of lead fingers, respectively.

25. The assembly of 18, wherein said first voltage reference plane and said second voltage reference is separated from said at least said first group of lead fingers and said second group of lead fingers, respectively, by an insulating adhesive structure.

26. The assembly of 25, wherein said insulating adhesive structure comprises an insulating film having an adhesive on opposing surfaces thereof, one surface of said opposing surfaces being adhered to at least one of said first group of lead

fingers and said second group of lead fingers and another surface of said opposing surfaces being adhered to at least one of said first voltage reference plane and said second voltage reference plane.

To further clarify the teaching wherein at least one of said first voltage reference plane and said second voltage reference plane includes projections extending away from a direction of said immediate proximity of said first group of lead fingers and said second group of lead fingers, respectively, it is noted that the planes are three dimensional; therefore, they project in all directions; hence, they include projections extending in all directions, including away from a direction of the immediate proximity of the first group of lead fingers and the second group of lead fingers, respectively.

To further clarify the teaching wherein said first voltage reference plane and said second voltage reference plane are of sufficient mass to measurably alter heat transfer characteristics of said assembly, it is noted that this is an inherent property of the planes.

However, Lee does not appear to explicitly teach the first voltage reference plane overlying at least a turning portion of the first group of lead fingers, the second voltage reference plane overlying at least a turning portion of the second group

of lead fingers, and the first group of lead fingers and the second group of lead fingers respectively extend to another, single side of the lead frame.

Nonetheless, at column 2, line 52 to column 4, line 15, Farnworth teaches a first group of lead fingers 23 BRO and a second group of lead fingers 23 BLO to respectively extend from first and second opposing sides of a semiconductor die 41 attached to a die-attach location on a lead frame to another, single side of the lead frame in a substantially mutually parallel configuration, and a turning portion of the first and second group of lead fingers. Furthermore, it would have been obvious to combine the products of Lee and Farnworth because, as cited, Lee teaches that, "The method provides for the fabrication of a low impedance package using a conventional lead frame," "the invention could readily be applied to any one of a variety of lead frame configurations," "the organization of the various leads will vary among packages. Many other arrangements will be apparent," and, "[the invention] uses presently available lead frames"; and the combination would provide a low impedance package using the conventional lead frame of Farnworth.

Also, Lee does not appear to explicitly teach the following:

2. The assembly of 1, wherein said lead frame comprises a vertical surface mount package configuration.

Nevertheless, as cited, Farnworth teaches wherein all of the lead fingers of the lead frame are configured to exit the package for external connection along a single side or edge of the package - as applicant defines the term *vertical surface mount package configuration* at specification page 8, lines 18-22 - therefore, Farnworth teaches wherein a lead frame comprises a vertical surface mount package configuration. Moreover, it would have been obvious to combine the product of Farnworth with the product of Lee for the same reasons recited supra.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Lee and Farnworth as applied to claims 1-10 and 13-26, and further in combination with Higgins (5583377).

As cited, in the combination, Lee teaches the following:
11. The assembly of 10, further comprising a packaging material 34 extending over at least one of said first voltage reference plane and said second voltage reference plane.

However, the combination of Lee and Farnworth does not appear to explicitly teach the following:
11. The assembly of 10, further comprising wherein said projections extend through said packaging material.

12. The assembly of 11, wherein said projections extend through said packaging material to an exterior surface thereof.

Nonetheless, at column 5, lines 32-42, and column 9, lines 2-9, Higgins teaches a packaging material 42, 54 extending over a voltage reference plane, wherein projections extend through the packaging material to an exterior surface thereof. In addition, it would have been obvious to combine the product of Higgins with the product of the combination of Lee and Farnworth because it would facilitate heat dissipation.

Applicant's remarks filed 8-21-2 have been fully considered and rendered moot by the rejection supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
Primary Examiner

Art Unit 2827

D.G.
22-Oct-02